

REMARKS

Claims 1-12 and 40-46 are pending. By this Amendment, claims 1, 4-6, 11 and 12 are amended, claims 13-16 are canceled, and claims 40-46 are added. The claims are amended to even more clearly distinguish over the applied references. No new matter is added by the above amendments.

Claims 1, 2, 4 and 5 stand rejected under 35 U.S.C. §103(a) over U.S. Patent No. 5,631,701 to Miyake in view of U.S. Patent No. 6,661,451 to Kijima et al. This rejection is respectfully traversed.

The combination of Miyake and Kijima et al. does not disclose or suggest the combination of features recited in independent claims 1 and 4. Independent claims 1 and 4 recite a first image processing circuit/instruction that creates a first image data, a first memory device in which the first image data is temporarily stored, a second image processing circuit/instruction that processes the first image data stored in the first memory device in units of blocks each ranging over n lines \times m rows, in which n and m each are equal to or greater than 2, in block sequence to create a second image data, and performing recording processing on the second image data.

The Office Action asserts that the signal processor 110 of Miyake corresponds to the claimed first image processing circuit, the frame memory 118 corresponds to the claimed memory device for temporarily storing image data, and the Y/C processor 114 corresponds to the claimed second image processing circuit. However, the Miyake signal processor 110 does not create first image data that is temporarily stored in frame memory 118, and which is then processed by the Y/C processor 114 of Miyake. Thus, Miyake does not disclose or suggest the arrangement of claims 1 and 4 in which a first image processing pre-treats image data to create first image data that is temporarily stored in a first memory device, and a second image processing processes the first image data stored in the first memory device to create a second

image data. In addition, Y/C processor 114 of Miyake does not correspond to the second image processing circuit/instruction of claims 1 and 4 because it does not process image data in units of blocks each ranging over n lines \times m rows, where n and m each are equal to or greater than 2, in block sequence. The Office Action asserts that "the Y/C conversion [performed by processor 114 of Miyake] will occur on a minimum of one complete RGB pair (i.e., a $n \times m$ block where $n = m = 1$).\" See the last two lines on page 3 of the Office Action. Even if the Office Action's assertion is correct, processor 114 of Miyake does not process image data in block sequence in which each block has the values n and m that are equal to or greater than 2. Kijima et al. does not overcome these deficiencies in Miyake.

Accordingly, independent claims 1 and 4, as well as their dependent claims, are patentable over Miyake in view of Kijima et al. Withdrawal of the rejection is requested.

Claims 3 and 6 stand rejected under 35 U.S.C. §103(a) over Miyake in view of Kijima et al., and further in view of U.S. Patent No. 4,774,565 to Freeman. This rejection is respectfully traversed. Freeman does not overcome the deficiencies in Miyake and Kijima et al. discussed above with respect to independent claims 1 and 4. Accordingly, claims 3 and 6 are patentable for at least the same reasons set forth above with respect to independent claims 1 and 4. Withdrawal of the rejection is requested.

Claims 7-10 stand rejected under 35 U.S.C. §103(a) over U.S. Patent No. 5,414,464 to Sasaki in view of U.S. Patent No. 5,778,106 to Juenger et al.¹ This rejection is respectfully traversed.

The combination of Sasaki and Juenger et al. does not disclose or suggest the combinations of features recited in independent claims 7 and 9. Independent claims 7 and 9

¹ Based upon the Form PTO-892 and the reference enclosed with the Office Action, it is believed that the Sasaki referred to in the Office Action is U.S. Patent No. 5,414,464, and not U.S. Patent No. 6,289,127, which was identified in item 7, page 6 of the Office Action.

recite that interpolation processing and low pass filtering processing are simultaneously performed on a color difference signal using filter coefficients for interpolation/low pass filtering. The Office Action recognizes that Sasaki does not disclose or suggest this simultaneous processing. The Office Action, however, asserts that the median filtering processing described at col. 7, line 29 – col. 8, line 13 of Juenger et al. includes both interpolation and low pass filtering. Applicants respectfully submit that the Office Action is incorrect. As explained at col. 7, lines 29-41 of Juenger et al., the median filter takes a series of pixels (9 pixels in the embodiment illustrated in Fig. 3(ii)) and replaces the pixel at the center of the filter region with a value that is the average of all pixels within the region. This does not correspond to performing interpolation processing and low pass filtering processing simultaneously using filter coefficients for interpolation/low pass filtering, as recited in claims 7 and 9. No coefficients are used in the median filter of Juenger et al. Rather, the median filter simply determines the average of a plurality of pixels and substitutes that average for one of the pixels.

Accordingly, independent claims 7 and 9, along with their dependent claims 8 and 10, are patentable over Sasaki and Juenger et al. Withdrawal of the rejection is requested.

Claims 11-16 stand rejected under 35 U.S.C. §103(a) over AAPA in view of U.S. Patent No. 4,774,565 to Freeman and U.S. Patent No. 5,153,730 to Nagasaki et al. This rejection is moot with respect to canceled claims 13-16 and is respectfully traversed with respect to claims 11 and 12.

In rejecting independent claim 11, the Office Action asserts that "if the median processing [of Freeman] is applied to the entire image as taught by Freeman, the median processing would naturally 'correspond to an $n \times m$ pixel area block during said format processing' as claimed." Applicants respectfully disagree.

Freeman discloses median processing during the creation of Y-G and C-G difference signals that are supplied to a reconstructing network 40 in order to derive for each pixel a signal value for each of the three colors while reducing color fringing artifacts. See, for example, col. 5, line 30 – col. 7, line 65 of Freeman. This does not correspond to the claim 11 second image processing circuit that performs format processing appropriate for data compression by engaging in median processing on first image data corresponding to an $n \times m$ pixel area block during the format processing, in which n and m each are equal to or greater than 2, as recited in claim 11. Accordingly, claim 11 and its dependent claim 12 are patentable over the combination of AAPA, Freeman and Nagasaki et al. Withdrawal of the rejection is requested.

In view of the foregoing, Applicants respectfully submit that this application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe anything further would be desirable to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,



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MAC/ccs

Attachment:
Petition for Extension of Time

Date: August 23, 2005

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